REMARKS

No claims have been amended. No new matter is included. Claims 1-37 are now pending in this application.

Claims 1-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Koizumi et al. (U.S. Patent No. 6,661,459)("Koizumi") in view of Fossum et al. (U.S. Patent No. 5,055,900)("Fossum"). The rejection is respectfully traversed.

The present invention relates to a pixel cell having a reduced potential barrier in a region where a gate and photodiode are in close proximity to one another. The present invention includes a gate of a transistor being formed at least partially below a surface of the substrate and a photodiode adjacent to the gate.

Koizumi relates to a solid state image pickup device. Koizumi at column 2, lines 60-63. Koizumi's device included a pixel having transistors, including transfer and reset transistors. Koizumi at column 4, lines 16-30; FIG. 3.

Fossum relates to a charge-coupled device formed by first defining relatively deep trenches having relatively small lateral dimensions in the surface of a silicon bulk region. Fossum at column 3, lines 3-27. Fossum specifically teaches electrode layers for the capacitors are formed in the trenches. Id.

Claim 1 recites, *inter alia*, "a gate of a transistor formed at least partially below a surface of the substrate, the gate having a bottom surface below the surface of the substrate; [and] a channel region of the transistor located below the bottom surface of the gate." Claim 20 recites, *inter alia*, "a gate of a transistor at least partially in the trench; [and] a channel region of the transistor formed below the trench." As agreed by the Office Action, Koizumi fails to disclose, teach or suggest such limitations.

The Office Action seeks to overcome these deficiencies by suggesting the combination of Fossum. Like Koizumi, Fossum does not teach or suggest "a gate of a transistor formed at least partially below a surface of the substrate, the gate having a bottom surface below the surface of the substrate; [or] a channel region of the transistor located below the bottom surface of the gate." Instead, Fossum relates to gate controlled capacitors. Thus, the cited combination of Koizumi and Fossum do not teach or suggest the limitations of claims 1 and 20. Claims 2-19 depend from claim 1 and are allowable along with claim 1. Claims 21-23 depend from claim 20 and are allowable along with claim 20.

Additionally, one of ordinary skill in the art would not have been motivated to combine the teachings of Koizumi and Fossum in the manner suggested by the Examiner. In essence, the Examiner has used the present specification as a roadmap attempting to construct the claimed invention from the references based on hindsight. The Examiner states that one of ordinary skill in the art would have been motivated to combine Koizumi and Fossum to "provide a longer path length for the photogeneration of carriers" and "to improve packing density." Office Action at 3. However, Fossum's teachings are particular to the use of capacitors and Koizumi is cited solely for the fact that it is a transistor. There is no reason evidenced in the references themselves to suggest combining together their teachings. Thus, the Examiner's suggested combination provides no such basis for combination to achieve the claimed invention. Those of ordinary skill in the art would not have been so motivated.

Accordingly, Koizumi in view of Fossum fails to establish a prima facie showing of obviousness. For at least the reasons set forth above as well as others, Applicants respectfully request the withdrawal of this rejection.

Claims 24-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Koizumi in view of Fossum as applied to claims 1-23, and further in view of Furumiya et al. (U.S. Patent No. 6,639,293)("Furumiya"). The rejection is respectfully traversed.

Like claims 1 and 20, claim 24 recites a pixel comprising, *inter alia*, "a gate of a transistor formed at least partially below a surface of the substrate, the gate having a bottom surface below the surface of the substrate, [and] a channel region of the transistor located below the bottom surface of the gate." As set forth above, Koizumi and Fossum, even when considered in combination, fail to teach or suggest such limitations. Additionally, one of ordinary skill in the art would not have been motivated to combine Koizumi and Fossum. Furumiya is cited, by the Office Action, for teaching an analog signal processor. However, Furumiya does not teach or suggest "a gate of a transistor formed at least partially below a surface of the substrate, the gate having a bottom surface below the surface of the substrate, [or] a channel region of the transistor located below the bottom surface of the gate." Thus, the cited combination fails to teach or suggest all limitations of the claim 24 invention. Claims 25-37 depend from claim 24 and are allowable along with claim 24.

For at least the reasons set forth above as well as others, Koizumi, Fossum and Furumiya, even considered in combination, fail to establish a prima facie case of obviousness under § 103(a). Accordingly, Applicants respectfully request that the rejection be withdrawn and the claims allowed.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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